Abstracts

A Low Noise AiGaAs/GaAs FET with P/sup +/-Gate and Selectively Doped Structure

K. Ohata, H. Hida, H. Miyamoto, M. Ogawa, T. Baba and T. Mizutani. "A Low Noise AiGaAs/GaAs FET with P/sup +/-Gate and Selectively Doped Structure." 1984 MTT-S International Microwave Symposium Digest 84.1 (1984 [MWSYM]): 434-436.

A low noise AIGaAs/GaAs FET with p/sup +/-gate and selectively doped structure has been developed. The FET utilizing a two dimensional electron gas has a closely spaced electrode planar structure on an MBE wafer. A 0.5 µm gate FET exhibited marked room temperature performances of 310 mS/mm transconductance and 1.2 dB noise figure with 11.7 dB associated gain at 12 GHz.

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